PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Charles A. MILLER — Art Unit: 3729

Application No: 09/819,181 — Examiner: Rick K. Chang

Filed: March 27, 2001

For: METHOD FOR FABRICATING AN IC INTERCONNECT SYSTEM INCLUDING AN IN-STREET INTEGRATED CIRCUIT WAFER VIA

SCHEDULE OF AMENDMENTS

The Title:

Please amend the title to read as follows:

METHOD FOR FABRICATING AN IC INTERCONNECT SYSTEM INCLUDING AN IN-STREET INTEGRATED CIRCUIT WAFER VIA

In the Claims:

Claims 13-18, rewrite as follows:

13. (Amended) A method for fabricating an interconnect system for providing a signal path to a first circuit node of an integrated circuit (IC) [contained on] formed within and on a portion of a semiconductor wafer having horizontal upper and lower surfaces, the method comprising the steps of:

a. forming a hole extending vertically through an area of the semiconductor wafer adjacent to the portion of the wafer containing the IC, and

b. placing a first conductive material in the hole, the first conductive material vertically extending through the hole, and

c. conductively linking the first conductive material to the first circuit node.

14. (Amended) The method in accordance with claim 13 further comprising [the] a step of:

d. cutting [on] the semiconductor wafer vertically along a horizontal saw-line extending across the hole such that [the] a portion of the semiconductor wafer containing the IC includes a peripheral edge formed along the saw-line upon which a portion of the first conductive material placed in the hole remains attached.

15. (Amended) The method in accordance with claim 14 further comprising [the] a step of:

e. forming a bond pad on the lower surface of the semiconductor wafer conductively linked to the [conductor] conductive material placed in the hole.

16. (Amended) The method in accordance with claim 14 [wherein the conductive material placed on the wafer at step b also extends from the hole horizontally along and attached to the lower surface of the semiconductor wafer under the portion of the semiconductor wafer containing the IC] further comprising a step of:

e. providing second conductive material extending horizontally from the first conductive material along and attached to the lower surface of the semiconductor wafer under the portion of the semiconductor wafer containing the IC.

17. (Amended) The method in accordance with claim 14 [wherein the conductive material placed on the wafer step b also extends from the hole horizontally along the upper surface of the semiconductor wafer on the portion of the semiconductor wafer containing the IC] wherein step c comprises a step of:

e. providing second conductive material extending horizontally on the upper surface of the semiconductor wafer and on the IC from the first conductive material to the first circuit node.

18. (Amended) The method in accordance with claim 17 [wherein the conductive material placed on the wafer at step b also extends from the hole horizontally along the lower surface of the semiconductor wafer on the portion of the semiconductor wafer containing the IC] further comprising a step of:

f. providing third conductive material extending horizontally from the first conductive material along and attached to the lower surface of the semiconductor wafer under the portion of the semiconductor wafer containing the IC.

In the Abstract:

Amend the abstract to read as follows:

[Vertical] A method for forming an integrated circuit (IC) interconnect system is described in which vertical holes are created in streets separating individual integrated circuit [(IC) dies] IC dice formed on a semiconductor wafer[, the]. The holes [spanning]

span saw-lines along which the wafer is to be later cut to separate the IC die from one another to form individual IC chips. The holes are then filled with conductive material. After the wafer is cut along the saw-lines, portions of the conductive material on opposing sides of the saw-lines remain on peripheral edges of the IC chip to form signal paths between the upper and lower surfaces of the IC chips.